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(54) Title of the Invention: Inter-LSI Connection Test Circuit
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(57) [Abstract]
[Objective] To reduce a connection test time by easily locating a connection error in the connection test between two LSIs in which there are a pair of inter-LSI signals output from an LSI-A10 to an LSI-B20 and provided from the LSI-B20 to the LSI-A10.
[Constitution] The inter-LSI connection test circuit includes a test data register 2 that inverts an inter-LSI signal provided from an LSI-B20 to an LSI-A10 and stores the inverted signal, a comparison register 4 that stores an inverted version of an output signal of the register 2, a comparator 5 that compares the contents of the register 2 and the contents of the register 4, and a loop (12, 6, 7) including the test data register 2, for transmitting data through the LSI-A10 and the LSI-B20, inverting the data, and returning the inverted data to the test data register 2.

[CLAIMS]
[Claim 1] 1. An inter-LSI connection test circuit, comprising:

an input signal inverting means that inverts a signal;

a test data storage means that stores an inverted signal from the input signal inverting means as test data;

a signal transfer means that returns the test data from the test data storage means to said input signal inverting means via an external integrated circuit;

a comparison and storage means that inverts and stores the contents of said test data storage means; and

a comparison means that compares the test data from

said test data storage means and the contents from said comparison and storage means.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD OF THE INVENTION]

The present invention is directed to a circuit that tests the connection between LSIs.

[0002]

[PRIOR ART] A conventional inter-LSI connection test that tests whether or not an inter-LSI signal is connected correctly is performed as described below. That is, the connection test is performed by a logical operation test and it is judged from the presence of a malfunction that the connection is acceptable or unacceptable.

[0003] Even if a malfunction can be found in a logical operation by a logical operation test in this manner, it is difficult to locate that the malfunction is a fault of the LSI itself or an inter-LSI connection error. In particular, if the logic of the LSI is complicated, there is a defect that much time is required in an analysis for specifying a signal line causing a connection error.

[0004]

[OBJECT OF THE INVENTION] The object of the present invention is to provide an LSI-connection test circuit that easily locate a connection error.

[0005]

[CONSTRUCTION OF THE INVENTION] An inter-LSI connection test circuit according to the present invention includes an input signal inverting means that inverts a signal, a test data storage means that stores an inverted signal from the input signal inverting means as test data, a signal transfer means that returns the test data from the test data storage means to said input signal inverting means via an external integrated circuit, a comparison and storage means that inverts and stores the contents of said test data storage means, and a comparison means that compares the test data from said test data storage means and the contents from said

comparison and storage means.

[0006]

[EMBODIMENTS] One embodiment of the present invention is described below in detail with reference to the drawing.

[0007] Referring to Fig. 1, there are an LSI-A10 and an LSI-B20. The LSI-A10 includes an input buffer 1 that inverts a signal supplied from the LSI-B20 via a line 104, a test data register 2 that stores an inverted signal supplied from the input buffer 1 via a line 105, a signal inverting circuit 3 that inverts test data output from the register 2 via a line 107, and a comparison register 4 that stores inverted test data supplied from the signal inverting circuit 3 via a line 106.

[0008] A comparator 5 compares the test data from the test data register 2 and the inverted test data from the comparison register 4. As a result of the comparison, for example, "0" is output to a line 109 when a comparison result is a match, and "1" is output to the line 109 when a comparison result is a mismatch.

[0009] An inter-LSI signal output selector 6 outputs the test data supplied from the register 102 via the line 107 to the line 103 when a test mode signal supplied via a line 111 is "1", and outputs a logical operation signal from the line 101 to the line 103 when the test mode signal is "0".

[0010] The LSI-B20 includes an inter-LSI signal output selector 7 that selects a selector output signal supplied from the LSI-A10 via the line 103 or a logical operation output signal supplied via the line 102 in accordance with the test mode signal supplied via the line 111.

[0011] The contents of the test data register 2 and the comparison register 4 are reset by a reset signal supplied via a line 110.

[0012] The operation of one embodiment of the present invention is described below in detail with reference to the drawing.

[0013] First, the test mode signal "1" is supplied to the line 111. Then, the register reset signal "1" is supplied to the line 110. The contents of the test data register 2 and

the comparison register 4 are reset in response to the reset signal. After this resetting, the register reset signal supplied via the line 110 is set to "0".

[0014] When the line for transferring an inter-LSI signal between the LSI-A10 and the LSI-B20 is connected correctly, the following operation is performed. That is, the selector 6 selects test data supplied from the test data register 2 via the line 107 and the selector 7 selects a selection result of the selector 6 provided via the line 103. As the result, the test data of the test data register 2 is provided to the input buffer 1 via the selector 6, the line 103, the selector 7, and the line 104 and stored in the test data register 2 via the line 105.

[0015] On the other hand, the test data output from the test data register 2 via the line 107 is inverted by the signal inverting circuit 3 and stored in the comparison register 4 via the line 106. The comparator 5 compares the data stored in the comparison register 4 and the data stored in the test data register 2.

[0016] When all of the aforementioned circuits operate normally, the comparator 5 outputs the signal "0" indicating a comparison match to the line 109.

[0017] If either of the lines 103 and 104 that connect the LSI-A10 and the LSI-B20 is disconnected, the signal supplied to the input buffer 1 is always set to "1". As the result, the test data supplied from the input buffer 1 and stored in the test data register 2 via the line 105 is always set to "1".

[0018] On the other hand, because this test data is inverted by the signal inverting circuit 3, the data stored in the comparison register 4 is always set to "0". Accordingly, in the comparator 5, the comparison always mismatches and the signal "1" is output to the line 9.

[0019] Alternatively, if the signal supplied to the input buffer 1 is always set to "0" due to the disconnection of either of the lines 103 and 104, the data supplied from the input buffer 1 to the test data register 2 via the line 5 is always set to "0".

[0020] On the other hand, this test data is inverted by the signal inverting circuit 3 and the signal supplied to the comparison register 4 is always set to "0". Accordingly, the comparator 5 outputs a signal "1" indicating the mismatch to the line 109.

[0021] That is, when either of the lines 103 and 104 for transferring an LSI signal is connected correctly, the matched output "0" of the comparator 5 is output to the line 109. when at least one of the lines 103 and 104 is disconnected, the mismatched output "1" is output to the line 109.

[0022] As this result, it can be judged whether an inter-LSI connection state is acceptable or unacceptable according to the output of the comparison result supplied to the line 109.

[0023]

[EFFECTS OF THE INVENTION] The present invention has such composition that the test data output from an LSI-A10 to an LSI-B20 returns to the original LSI-A10 through a bus from the LSI-B20 to the LSI-A10 between two LSIs in which there is a pair of the inter-LSI signals output from the LSI-A10 to the LSI-B20 and provided from the LSI-B20 to the LSI-A10 and an inter-LSI connection test can be performed every two inter-LSI signal lines. There is an effect that a test time can be reduced because this test can easily locate a connection error.

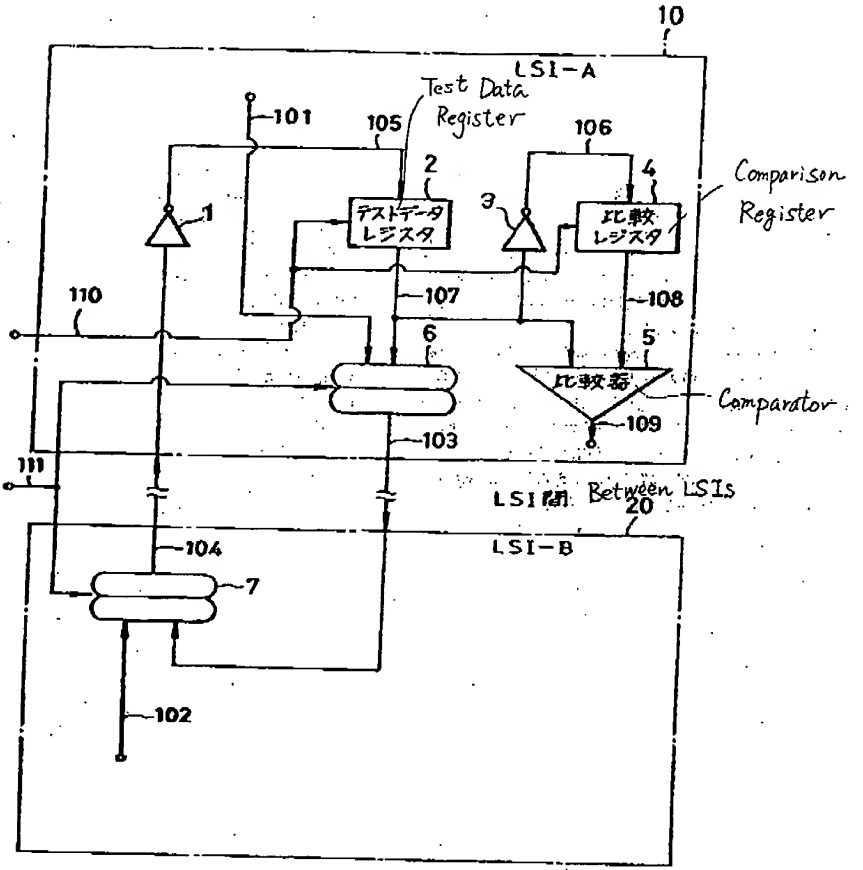
[BRIEF DESCRIPTION OF DRAWINGS]

Fig. 1 is a drawing showing one embodiment of the present invention.

[EXPLANATION OF REFERENCE NUMERALS]

1. Input Buffer
2. Test Data Register
3. Signal Inverting Circuit
4. Comparator Register
5. Comparator
6. Selector
7. Selector

【図1】


10
LSI-A
Test Data Register
101
105
106
2
4
Comparison Register
1
3
テストデータレジスタ
比較レジスタ
110
107
108
6
5
比較器
Comparator
109
103
111
LSI間 Between LSIs
20
LSI-B
104
7
102